Claims

[c1] 1. A method of forming a layer of Si comprising:
providing a substrate having semiconducting regions separated by insulating regions;
implanting dopants into said substrate to provide an etch differential doped portion in said semiconducting regions underlying an upper Si-containing surface of said semiconducting regions;
forming a trench in said substrate including portions of said semiconducting regions and said insulating regions;
removing said etch differential doped portion from said semiconducting regions to produce a cavity underlying said upper Si-containing surface of said semiconducting regions;
passivating exposed Si-containing surfaces underlying said upper Si-containing surface of said semiconducting regions, wherein said exposed Si-containing surfaces underlying said upper Si-containing surface are formed by said cavity; and
filling said trench with a trench dielectric, wherein said dielectric material encloses said cavity underlying said upper Si-containing surface of said semiconducting regions.

[c2] 2. The method of Claim 1 wherein said upper Si-containing surface of said semiconducting regions has a uniform thickness of less than about 100 Å.

[c3] 3. The method of Claim 1 wherein said providing a semiconducting substrate having semiconducting regions separated by insulating regions comprises:
forming an etch mask protecting a portion of said substrate, wherein an

exposed portion of said substrate is unprotected;

etching said exposed portion of said substrate to form isolation regions, wherein a remaining portion of said substrate forms said semiconducting regions; and

depositing insulating material within said isolation regions to form insulating regions.

[c4] 4. The method of Claim 3 wherein said insulating material is an oxide, nitride, or oxynitride deposited using chemical vapor deposition.

[c5] 5. The method of Claim 1 wherein said implanting dopants into said semiconducting regions comprises ion implanting an etch differential dopant into at least said semiconducting regions, wherein said etch differential dopant comprises Ar, As, P, B, or H.

[c6] 6. The method of Claim 3 wherein said implanting is conducted using an implant energy ranging from about 1 keV to about 100 keV and an implant concentration ranging from about $1x10^{14}$ atoms/cm^2 to about $1x10^{17}$ atoms/cm^2.

[c7] 7. The method of Claim 1 wherein said removing said etch differential doped portion comprises a highly selective etch process comprising $HF:HNO_3:CH_3COOH$, ethylenediamine-pyrocatechol-water, KOH, a mixture of $NH_4OH/H_2O_2/H_2O$, a mixture of $HCl/H_2O_2/H_2O$ or combinations thereof.

[c8] 8. The method of Claim 1 wherein said passivating said exposed Si-containing surfaces provides a passivation layer underlying said upper Si-containing surface of said semiconducting regions, said passivation layer having a thickness ranging from about 30 Å to about 100 Å.

[c9] 9. The method of Claim 8 wherein said passivation layer underlying said upper Si-containing surface is formed via thermal oxidation, said thermal oxidation having an annealing temperature ranging from about 800°C to 1000°C.

[c10] 10. The method of Claim 1 wherein said forming said trench in said substrate including said semiconducting regions and said insulating regions comprises:
forming an trench patterned etch mask atop said substrate, wherein said trench patterned etch mask defines a trench region of said substrate; and
etching said trench region to provide a trench.

[c11] 11. The method of Claim 1 wherein said trench dielectric comprises an oxide, a nitride, or an oxynitride deposited by high density plasma chemical vapor deposition or plasma enhanced chemical vapor deposition.

[c12] 12. The method of Claim 1 wherein said substrate comprises Si, SiGe, SiGeC, SiC, or combinations thereof.

[c13] 13. A method of forming a layer of Si comprising:
providing a substrate having semiconducting regions separated by insulating regions;
forming a block mask protecting a portion of said substrate, where an unprotected portion of said substrate is exposed;
implanting dopants into said unprotected portion of said substrate to provide an etch differential doped portion in said semiconducting regions underlying an upper Si-containing surface of said semiconducting regions;
forming a trench in at least said unprotected portion of said substrate

including said semiconducting regions and said insulating regions;
removing said etch differential doped portion from said semiconducting regions to produce a cavity underlying said upper surface of said semiconducting regions; and
filling said trench with a trench dielectric, wherein said dielectric material encloses said cavity underlying said upper Si-containing surface of said semiconducting regions.

[c14] 14. The method of Claim 13 wherein said upper Si-containing layer has a uniform thickness of less than about 100 Å.

[c15] 15. The method of Claim 13 wherein said implanting dopants into said semiconducting regions comprises ion implanting said etch differential dopant such as Ar, As, P, Ga, H, or B into said semiconducting regions.

[c16] 16. The method of Claim 13 wherein said etching said etch differential doped region comprises a highly selective etch comprising $HF:HNO_3:CH_3COOH$, ethylenediamine-pyrocatechol-water, KOH, a mixture of $NH_4OH/H_2O_2/H_2O$, a mixture of $HCl/ H_2O_2/H_2O$ or combinations thereof.

[c17] 17. The method of Claim 13 wherein said unprotected portion of said substrate is processed to provide silicon-on-insulator devices and a remaining portion of said substrate is processed to provide bulk-Si devices.

[c18] 18. A semiconducting structure comprising:
at least two insulating pillars atop a substrate;
a layer of Si bridging said at least two insulating pillars; and
a cavity formed between each of said two insulating pillars and underlying said layer of Si, wherein said layer of silicon has a uniform thickness of

about 10 nm or less.

[c19] 19. The semiconducting structure of Claim 18 wherein said layer of Si bringing said at least two insulating pillars further comprises a passivation layer underlying said layer of Si.

[c20] 20. The semiconductor structure of Claim 19 wherein said passivation layer has a thickness of 10 nm or less.